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WHITE PAPER:
ACE - Automated Circuit Extraction

Introduction: Where Did Engineering Design Go?

The traditional approach to RF/MW circuit design – which is the present day foundation for high-frequency wireless design applications – is being pressured simultaneously by an increase in operating frequencies / bandwidth and a decrease in physical footprint size. The result is that the physical design challenges faced by circuit designers are rapidly increasing, while choices for how these challenges should be best-addressed are not.

The drive to put more functionality into the same or smaller space is particularly demanding on the RF/microwave design flow because of the increased and unavoidable need to model interconnects and their interactions. Ideally, modeling all of the interactions at the schematic level, using distributed line, discontinuity, and coupled-line models (Figure 1) is preferred.

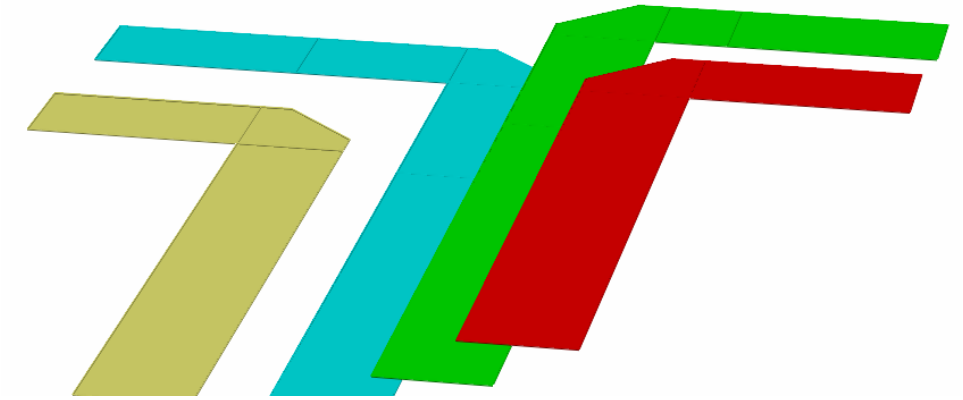

Figure 1 – layout of a distributed multi-layer coupled line structure with bend discontinuities

This is because, first and foremost, modeling each interconnect and interconnect interaction parametrically gives the design engineer the ability and control to predicatively design the circuit. These models then simulate very quickly, and, finally, fast-to-simulate parametric models enable tuning, optimization and design centering in a timely and interactive manner with today's modern design tools.

While there is nothing preventing an engineer from placing coupled-line models and discontinuities for all the schematic wires in an RF/MW circuit, the complexity of today's wireless designs makes this an unrealistic and unreasonable approach. Even for some simple, real world examples (Figure 2), this manual process is incredibly time-consuming and error-prone.

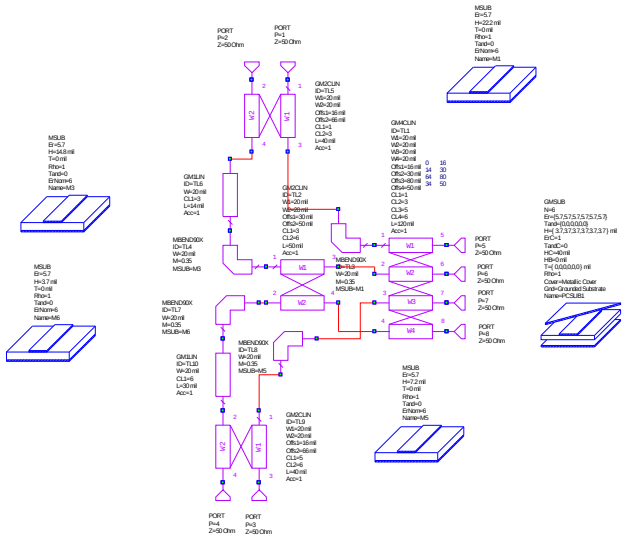

Figure 2 – Manually-created schematic representing Figure 1

Consequently, the engineer's response has been to forego design and go straight to analysis/verification as a weak, but faster, alternative. While this method saves engineering time by avoiding the manual insertion of various RF/MW line models, the trade-off is that the overall engineering time grows as the analysis/verification burden for using EM as a design tool has mushroomed. In other words, design simulation and modeling tools are time-consuming with regard to computational hours, and, as a result, engineers have traded extensive manual hours in favor of even more extensive computational hours for EM analysis of RF/microwave designs.

The reality has unfortunately become endless layout-EM-analysis cycles as lines are moved and vias replaced. This is all being done without any design engineering methodology, first-principles insight, or parametric handle into or behind the reasons for doing so. This situation is all the more critical when considering that by the time a layout is complete enough to do this sort of layout-EM-analysis cycle, the design is closer to the end of its cycle than the beginning. Study after study on the engineering of complex

systems, from spacecraft to software to electronics, shows that it is much more cost-effective to identify and fix design deficiencies as early as possible in the design cycle; doesn't this mean that the improper use of EM as a design tool makes this a costly and risky proposition to many RF/MW design flows?

What is ACE?

ACE™ automated circuit extraction technology from Applied Wave Research, Inc. (AWR®) is an innovative response to the overuse of EM as a design tool. ACE software reclaims parametric design for the user by creating netlist-based representations of complex interconnects using the very same networks of parametric models designers themselves would use if they had the time and patience to do so, in a fraction of the time that it would take EM tools to create S-parameters. The speed, accuracy, and parametric nature of ACE software enable engineers to return to real design by exploring design alternatives and changes in seconds. Obviously, EM is still a necessary part of the flow, but the ACE tool enables engineers to once again design rather than analyze, even on many of the most challenging RF/MW designs.

ACE software is based on the proven digital and analog-mixed signal technique of circuit extraction, but uses microwave models and principles. The tool puts the engineer back into the driver's seat of design by creating circuit models from layout geometries. The ACE tool, like all circuit extractors, creates a model for interconnects by geometrically analyzing a layout through breaking it down into pieces that the extractor understands, mapping each piece of the reduced geometry to a model, and then combining the models intelligently to create a simulatable representation. Digital and analog mixed-signal (AMS) extractors typically use RLCK models (Figure 3) to model interconnect-reduced geometries, but these require very dense networks at microwave frequencies to capture dispersion and skin-effect, and they tend to be bandwidth-limited.

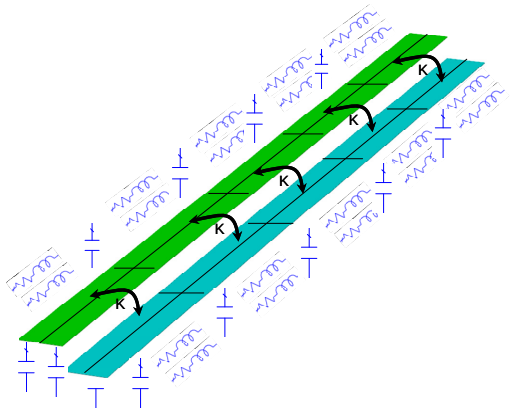

Figure 3 – Digital and AMS extractors model coupled transmission lines using dense networks of RLCK models

ACE software, on the other hand, views the layout in terms of distributed line, coupled-line, and discontinuity models (Figure 4) that microwave engineers have been using for years, such as MLIN/SLIN, MTEE/STEE, and M2CLIN/S2CLIN, and so dispersion, skin-effect, and bandwidth are non-issues. Moreover, vias can be modeled with S-parameter files from pre-defined via libraries.

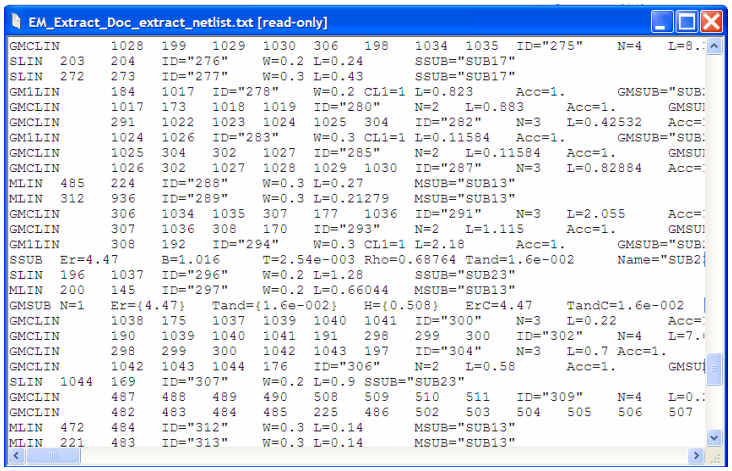

Figure 4 – ACE extracted netlist of an RF/microwave circuit. Extraction time is approximately 1 second for DC to 10GHz

The ACE tool generates the netlist in seconds for complex arrangements of interconnects that engineers would prefer to make, but either don't have the hours or days to do it or find it too error-prone, and/or where EM analysis would take days or even weeks for a single design iteration, provided the computer hardware didn't crash.

ACE software goes even a few steps further than this. As part of the way in which it views the schematics, the same ground planes that are assumed for substrate definitions are found and simplified so that lines separated by a ground plane are not grouped together in a coupled line structure. Even with low temperature co-fired ceramic (LTCC) materials, where dielectric constant and thickness may vary, ACE software defines on-the-fly substrate definitions for the distributed models it extracts. Also, for lines that crossover on different layers not separated by a ground plane, a coupling capacitor is calculated based on geometry. To obtain the highest degree of accuracy, the ACE tool can even be directed to extract geometries to models, which themselves have highly optimized, built-in, EM solvers. In many cases, the software can provide accuracy that is similar to EM analysis, but is hundreds if not thousands of times faster for design tasks early and throughout the design flow.

The ACE technology uses all of the models designers would use to model complex interconnects if they had the time and the patience. For fast, efficient, and accurate answers it uses closed-form models such as MLIN and SLIN for lines, MTEE for t-junctions, and M2CLIN for coupled lines. Without sacrificing speed, AWR's industry-leading X-models, EM table-based models with the accuracy of EM and the speed of closed-form models, can be used for discontinuities. For the most accurate answers, designers can direct the ACE tool to use models that have finite element method (FEM) solvers built right in that are highly optimized to solve that particular geometry. GFMCLIN, for example, has an FEM solver inside, which turns the parametric descriptions into geometries solved by its FEM solver in a fraction of the time of generalized, three-dimensional (3D) FEM tools. Designers now have the choice to trade off the difference between speed and degree of accuracy when they chose to have ACE use method-of-moments (MoM) solvers -- faster than the FEM-based circuit models such as GFMCLIN and more accurate than the closed-form models such as M2CLIN.

The same geometries that were sent to an EM solver in the past can now be sent to ACE. Throughout the design flow, ACE software can be used, in conjunction with EM-based discontinuity and coupled line models, to design and refine. The very same geometries that are sent to the ACE tool during design can then be sent, capacity permitting, to any one of the EM solvers (CST, Flomerics, Sonnet, or Zeland) integrated into AWR's EM Socket™ II tool for verification.

Real-World Examples of ACE

Example 1 – MMIC distributed amplifier design

A monolithic microwave integrated circuit (MMIC) distributed amplifier depends on the inter-stage interconnects to define its impedance and bandwidth characteristics. Figure 5 shows such a design using pseudomorphic high electron mobility transistor (PHEMT) technology initialed modeling the interconnects with distributed MLIN, MBEND, MTEE, etc. models, but, for example, no coupling among adjacent arms of the meandered interstage lines.

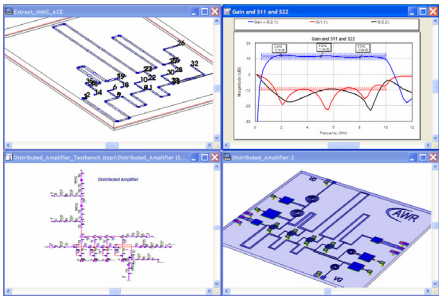

Figure 5 – Distributed amplifier with ACE to extract distributed and discontinuity models with no interconnect couplings. Extraction time is ~ 0.5 seconds for DC to 12GHz

Using ACE software with a very large coupling radius specified yields greater bandwidth, but at the expense of gain flatness; the culprit is the couplings, shown in extracted schematic form (Figure 6).

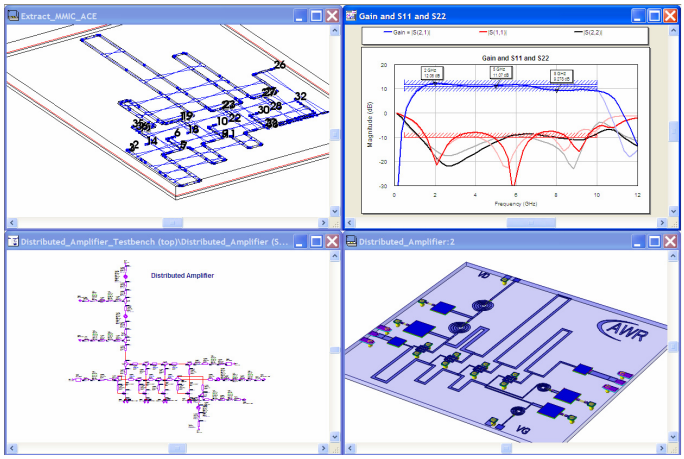

Figure 6 – ACE software with large coupling radius showing performance degradation. Extraction time is approximately 1 second for DC to 12GHz

By reducing the ACE coupling radius, it can be seen that majority of the detrimental coupling is due to the adjacent arms of the meandered interconnects (Figure 7).

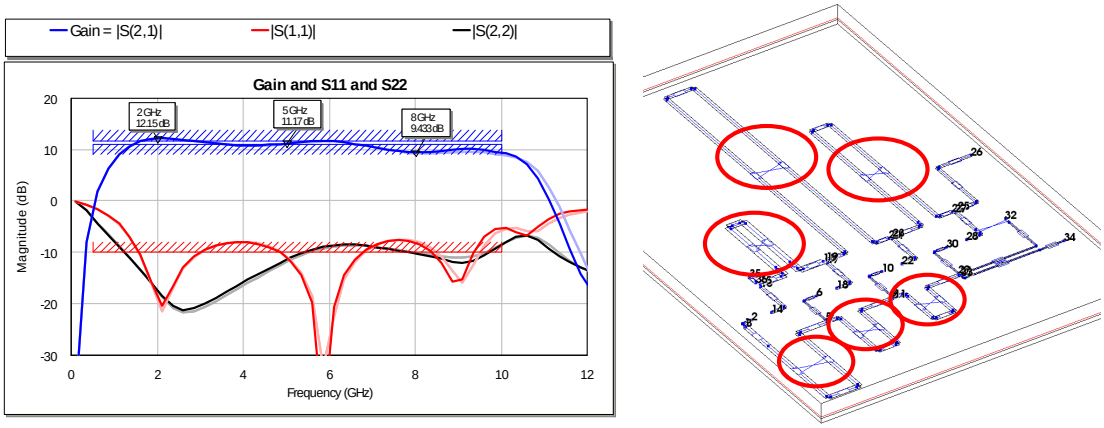

Figure 7 – Reduced ACE coupling radius (bold traces, left) reveals overall performance degradation (gray traces, left) mainly due to adjacent couplings (red circles, right)

In a matter of minutes, the ACE technology empowers the designer to identify, pinpoint, and redesign the circuit, whereas iterating with layout and EM analysis would likely take the better part of a day or days.

Example 2 – Module/printed circuit board (PCB) design problem

In this example, ACE capabilities are applied to a complex, 16-layer PCB application (Figure 8) early in the design flow in order to efficiently and accurately design the RF transmit signal path, shown here with the copper-colored power and ground planes as complete fills. The large transceiver chip requires a good deal of bypassing which adds more than a few nets to the control lines and RF signal path. All in all, at this stage of the design, the 16-layer board has approximately 75 nets, dozens of vias, and 160 ports.

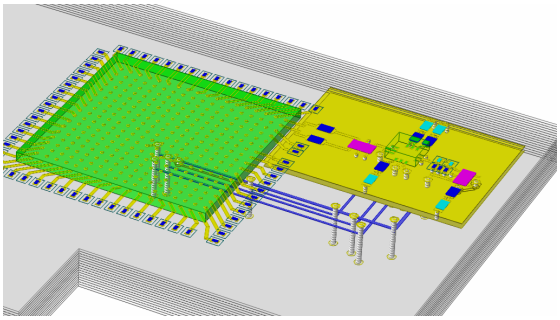

Figure 8 – 16-layer printed circuit board (PCB) worldwide interoperability for microwave access (WiMAX) with transceiver chip and RF transmit signal path

Analyzing this large a design with a 3D planar solver is a time-consuming task because of the time required to create the Green's function for the multiple, non-uniform layers. 3D FEM techniques would also take a long time -- even longer because of the amount of metal. Even 3D finite-difference time-domain **(**FDTD) software products would suffer due to the high port count. Using ACE with this design provides an answer in a little over one second when modeling all the coupled lines with the GMCLIN MOM models.

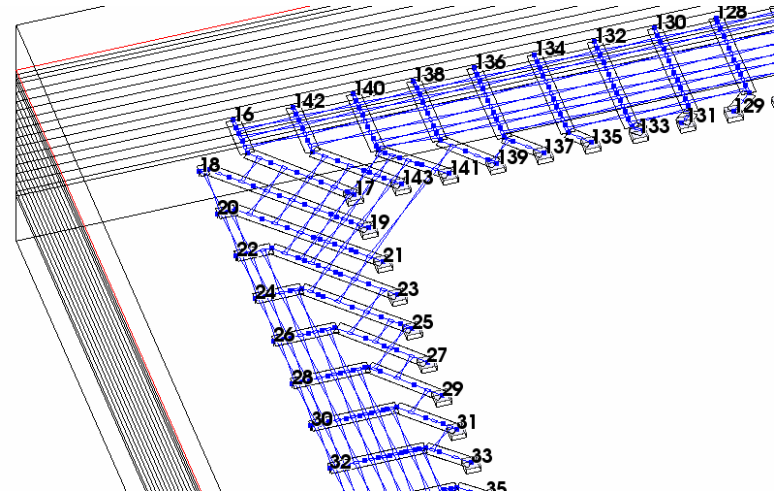

Figure 9 – ACE extracted view for transceiver bypass routing.
Extraction time is approximately 1.2 seconds using FEM-based models at 5.2GHz.

In the extracted view shown in Figure 9, the ACE tool decomposes parallel line segments into coupled-line models such that as nets that have some segment or trace become parallel or stop being parallel with other nets' segments, the software inserts a new coupled-line model in series with the original, with the difference between the two representing one more or one fewer coupled lines. The ACE software is capable of creating very dense networks of interconnects in this way by finding units, or portions, of the layout that can be grouped together based on the extensive library of models in the AWR design environment. These are the very same models that designers have been relying upon for nearly a decade to design RF/microwave circuits up to and beyond 100GHz.

Conclusion

Engineering design in recent years has become over-reliant on analysis because RF/microwave design tools have not kept pace with the challenges of next-generation design. AWR's ACE innovation puts the power of the design process back into the engineer's hands because it provides the user with the ability to parametrically investigate designs by combining the proven technique of circuit extraction with microwave models and understandings. The ACE technology identifies and fixes complex interconnect issues during the design process, where it is timely and cost-effective to do so, while at the same time reserving EM analysis for final verification of the design. Engineer's of the world, ACE your designs!